Appl'n 10/787,276
Annex I: Claims rejected over Hak correlated to Exhibit A of Rule 131 Declaration of Peter D. Brewer

Claims (including proposed amendments)	Exhibit A (report dated November 8, 2001), page 2
1. A method for removing defects from a semiconductor surface, comprising:	"a self-masking process for removing growth defects from the surface of the MBE grown Sb-based epilayers"
coating the semiconductor surface and the defects with a planar protective layer;	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"
thinning the planar protective layer to selectively reveal portions of the defects;	"dry-etching the resist layer to a thickness of ~0.5 microns (to reveal the tops of the defect structures but protecting the remainder of the semiconductor surface)"
removing the defects; and	"wet chemical etching of the exposed defect structures"
removing the planar protective layer.	"stripping of the remaining photoresist layer"
2. The method of claim 1 wherein the planar protective layer uniformly covers the defects.	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"
3. The method of claim 1 wherein the planar protective layer is a photoresist layer.	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"
4. The method of claim 3 wherein the photoresist layer has a thickness from about 5	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"

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to about 10 microns.	
5. The method of claim 4 wherein the photoresist layer has a thickness of about 8 microns.	"coating the surface of the wafer with a thick photoresist layer (5-10 microns)"
18. The method of claim 1, wherein removing of the defects is performed by etching.	"wet chemical etching of the exposed defect structures"
19. The method of claim 1, wherein thinning the planar protective layer is performed by a process which is identical to a process for removing the planar protective layer.	"stripping of the remaining photoresist layer"
20. The method of claim I, wherein the semiconductor surface comprises a semiconductor selected from a group consisting of GaSb, InAs, Si, InP; GaAs, InAs, and AlSb.	"a self-masking process for removing growth defects from the surface of the MBE grown Sb-based epilayers"
21. The method of claim 1, wherein the defects are removed using a wet chemical etchant.	"wet chemical etching of the exposed defect structures"

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Peter D. BREWER	Examiner: Thanhha S. Pham
Serial No.: 10/787,276	Art Unit: 2813
Filed: February 25, 2004	Our Ref: B-4712 620052-7
For: "SELF-MASKING DEFECT REMOVING METHOD"	Date: September 5, 2006
	Re: Declaration of Peter D. Brewer under 37 C.F.R. 1.131

DECLARATION OF PETER D. BREWER UNDER 37 C.F.R. § 1.131

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450a

I, Peter D. Brewer, declare and say:

1. I am the inventor named in the above-identified application.

2. I completed the invention disclosed and claimed in the above-identified application in the United States of America no later than November 8, 2001.

3. Exhibit A to this declaration is a copy of a "Progress, Status and Management Report" for research on "Antimonide Based Compound Semiconductors

(ABCS)" that I helped to prepare. The date of the report is stated on its cover: November 8, 2001. Irrelevant material has been redacted from the copy of the report attached as Exhibit A. The report evidences actual reduction to practice of the invention claimed in this application before November 8, 2001.

4. The "Description of Progress" on page two of the "Progress, Status and Management Report" attached as Exhibit A contains a section that I wrote. It describes research directed to a "substrate transfer technology focused on the preparation of the MBE grown epi-layer surfaces prior to wafer bonding and processes for selectively removing GaSb substrates after wafer bonding." "Morphological growth-defects on the surface of the Sb-based epilayers" are identified as problems because these defects "interfere with the bonding of the GaSb epilayers and the sapphire substrates." The solution was "a self-masking process for removing growth defects form the surface of the MBE grown Sb-based epilayers."

5. As stated in the "Progress, Status and Management Report" attached as Exhibit A, the "self-masking process" involves four processing steps: "1) coating the surface of the wafer with a thick photoresist layer (5-10 microns), 2) dry-etching the resist layer to a thickness of ~0.5 microns (to reveal the tops of the defect structures but protecting the remainder of the semiconductor surface), 3) wet chemical etching of the exposed defect structures, and 4) stripping of the remaining photoresist layer."

6. The "Progress, Status and Management Report" attached as Exhibit A observes that "this process effectively removes the protruding defect structures from the surface of the semiconductor wafer without [affecting] the surrounding epilayer

material." The "Report" notes the successful results of the process: "[i]nitial results using this process to prepare as-grown HBT wafers for bonding to sapphire substrates indicate enhanced bonding yields as a result of eliminating the morphological growth defects. In these experiments, bonding surface area yields as high as 94% were obtained."

I declare further that all statements made herein of my own knowledge are true; that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patents issuing thereon.

Date: September 5, 2006

Peter D. Brewer

Peter D. Brewer

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Progress, Status And Management Report

N660001-01-C-8033

CDRL A001

Antimonide Based Compound Semiconductors (ABCS)

November 8, 2001

Period Covered: October 1 2001 –November 1, 2001

Unclassified

SPAWAR Systems Center, San Diego

Application No.: 10/787,276
Exhibit A to Declaration of Peter D. Brewer

Description of progress

Work included establishing a wafer transfer process, and improvement of the performance of existing prototype ABCS-based HEMT and HBT devices.

Substrate Development:

The development of the substrate transfer technology focused on the preparation of the MBE grown epi-layer surfaces prior to wafer bonding and processes for selectively removing GaSb substrates after wafer bonding.

As reported in the previous progress report, morphological growth-defects on the surface of the Sb-based epilayers are found to interfere with the bonding of the GaSb epilayers and the sapphire substrates. The growth-defects and other particles found on the wafer surfaces, cause the bonding wafers to deform around them forming circularly un-bonded interface areas or voids. The un-bonded areas resulting from even small protuberances are fairly large, for example, a particle of ~1 micron diameter leads to an un-bonded area with a diameter of ~0.5 cm for GaSb and sapphire wafers. The defects are produced during the MBE growth of epilayers and are the result of effusion cell spitting or growth defects caused by impurities or surface imperfections on the original GaSb substrate wafer. The defects are an integral part of the semiconductor wafer surface and cannot be removed with conventional particulate removal processes. The density of defects on the wafer range from 1-100/cm^2 and range in size from 1-50 microns with heights typically from 1-10 microns.

HRL has developed a self-masking process for removing growth-defects from the surface of the MBE grown Sb-based epilayers. This process involves four processing steps: 1) coating the surface of the wafer with a thick photoresist layer (5-10 microns), 2) dry etching the resist layer to a thickness of ~0.5 microns (to reveal the tops of the defect structures but protecting the remainder of the semiconductor surface), 3) wet chemical etching of the exposed defect structures, and 4) stripping of the remaining photoresist layer. Although simple, this process effectively removes the protruding defect structures from the surface of the semiconductor wafer without effect the surrounding epilayer material. Initial results using this process to prepare as-grown HBT wafers for bonding to sapphire substrates indicate enhanced bonding yields as a result of eliminating the morphological growth-defects. In these experiments, bonding surface area yields as high as 94% were obtained.

A second area of this task focused on developing a process for selectively removing GaSb substrates from InAs epilayers after wafer bonding. This month's activity has centered on developing a three-step process to thin and selectively remove the GaSb substrate. The process includes the following steps: 1) lap and polish the GaSb substrate (bonded to sapphire) to a thickness of 50 microns, 2) continue thinning of the GaSb substrate material to ~20 microns using a selective wet chemical etch, and 3) remove thinned GaSb material from the InAs epilayers using a highly selective dry etch process. The multi-step process is used to efficiently remove the substrate material from the epilayer device structure and not over burden the dry etch system with excessively long etch runs. The dry etch process uses an inductively coupled plasma etch system using a Cl-based etch chemistry that has demonstrated etch selectively of 1000:1 for GaSb and InAs, respectively. This process was successful used to completely remove the GaSb substrate material from a InAs diode structure epilayer bonded to sapphire.

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